**IN THE CLAIMS:**

1. (currently amended) For use in a wide-issue pipelined processor, a mechanism for reducing pipeline stalls between conditional branches, comprising:

mispredict program counter (PC) queue ~~storage~~, configured to store multiple mispredict PC values, wherein each of said multiple mispredict PC values corresponds to a conditional branch instruction to enter into ~~in~~ a pipeline of said processor; and

a mispredict PC value selector configured to select one of said multiple mispredict PC values to move to staging registers to track a corresponding conditional branch instruction as said corresponding conditional branch instruction moves through stages of said pipeline, said select based on when said corresponding conditional branch instruction enters said pipeline.

2. (currently amended) The mechanism as recited in Claim 1 further comprising a mispredict PC generator configured to generate a mispredict PC value for each of said conditional branch instruction ~~in said pipeline~~.

3. (previously presented) The mechanism as recited in Claim 2 wherein said mispredict PC generator generates a branch prediction employed to prefetch instructions and said mispredict PC value in a single clock cycle.

4. (currently amended) The mechanism as recited in Claim 1 wherein said ~~mispredict PC storage includes a number of~~ staging registers and said a mispredict PC queue form a mispredict PC storage ~~configured to store said multiple mispredict PC values, said mispredict PC value selector configured to select said one of said multiple mispredict PC values from said mispredict PC queue to cause said selected one to move into said staging registers to track said corresponding conditional branch instruction~~.

5. (canceled)

6. (currently amended) The mechanism as recited in Claim 1 wherein said one of said multiple mispredict PC values tracks said corresponding conditional branch instruction by moving through said staging registers ~~of said mispredict PC storage~~ as said corresponding conditional branch instruction moves through said stages in said pipeline.

7. (currently amended) The mechanism as recited in Claim 4 ~~1~~ wherein said mispredict PC storage stores said each of said mispredict PC values at least until a resolution of said corresponding conditional branch instruction occurs in an execution stage of said pipeline.

8. (previously presented) The mechanism as recited in Claim 2 wherein said mispredict PC generator is configured to generate said mispredict PC value before branch instructions are grouped.

9. (currently amended) For use in a wide-issue pipelined processor, a method of reducing pipeline stalls between conditional branches, comprising:

storing multiple mispredict program counter (PC) values, wherein each of said multiple mispredict PC values corresponds to a conditional branch instruction to enter into ~~in~~ a pipeline of said processor;

selecting one of said multiple mispredict PC values to move to staging registers to track a corresponding conditional branch instruction as said corresponding conditional branch instruction moves through stages of said pipeline; and

basing said selecting on when said corresponding conditional branch instruction enters said pipeline.

10. (currently amended) The method as recited in Claim 9 further comprising generating a mispredict PC value for each of said conditional branch instruction ~~in said pipeline~~.

11. (previously presented) The method as recited in Claim 10 wherein said generating is carried out in a single clock cycle, said method further comprising generating a branch prediction in a single clock cycle.

12. (previously presented) The method as recited in Claim 9 wherein said selecting includes selecting one of said multiple mispredict PC values from a mispredict PC queue configured to store said multiple mispredict PC values.

13. (canceled)

14. (currently amended) The method as recited in Claim 9 wherein said one of said multiple mispredict PC values tracks said corresponding conditional branch instruction by moving through said staging registers ~~in a mispredict PC storage~~ as said corresponding conditional branch instruction moves through stages in said pipeline.

15. (previously presented) The method as recited in Claim 9 wherein said storing includes storing said each of said mispredict PC values at least until a resolution of said corresponding conditional branch instruction occurs in an execution stage of said pipeline.

16. (original) The method as recited in Claim 9 wherein said processor is a digital signal processor.

17. (currently amended) A digital signal processor, comprising:

a pipeline having stages capable of executing conditional branch instructions;

a wide-issue instruction issue unit;

mispredict program counter (PC) queue ~~storage~~, that stores multiple mispredict PC values, wherein each of said multiple mispredict PC values corresponds to a conditional branch instruction to enter into ~~in~~ said pipeline; and

a mispredict PC value selector that selects, based on when said corresponding conditional branch instruction enters said pipeline, one of said multiple mispredict PC values to move into staging registers to track said corresponding conditional branch instruction as said corresponding conditional branch instruction moves through said stages.

18. (currently amended) The DSP as recited in Claim 17 further comprising a mispredict PC generator that generates a mispredict PC value for each of said conditional branch instruction ~~in said pipeline~~.

19. (previously presented) The DSP as recited in Claim 18 wherein said mispredict PC generator generates a branch prediction employed to prefetch instructions and said mispredict PC value in a single clock cycle.

20. (currently amended) The DSP as recited in Claim 19 wherein said ~~mispredict PC storage includes a number of staging registers and mispredict PC queue that stores said multiple mispredict PC values, said~~ mispredict PC value selector is configured to select said one of said multiple mispredict PC values from said mispredict PC queue to cause said selected one to move through ~~into~~ said staging registers to track said corresponding conditional branch instruction.

21. (canceled)

22. (currently amended) The DSP as recited in Claim 17 wherein said one of said multiple mispredict PC values tracks said corresponding conditional branch instruction by moving

through said staging registers ~~in said mispredict PC storage~~ as said corresponding conditional branch instruction moves through said stages.

23. (currently amended) The DSP as recited in Claim 17 wherein said mispredict PC queue and said staging registers form a mispredict PC storage that stores said each of said mispredict PC values at least until a resolution of said corresponding conditional branch instruction and said resolution occurs in an execution stage of said pipeline.

24. (currently amended) The mechanism as recited in Claim 1 ~~4~~ wherein said mispredict PC queue ~~of said mispredict PC storage~~ has at least one more slot than said number of said staging registers.

25. (currently amended) The method as recited in Claim 9 ~~12~~ wherein said mispredict PC queue ~~of said mispredict PC storage~~ has at least one more slot than a number of staging registers employed with said storing.

26. (currently amended) The DSP as recited in Claim 17 ~~20~~ wherein said mispredict PC queue ~~of said mispredict PC storage~~ has at least one more slot than said number of said staging registers.